IN THE CLAIMS

Please cancel claims 1, 2, 4, 5 and 7, 8, 10 and 11 without prejudice or disclaimer.

Please amend claims 3, 6, 9 and 12 as indicated below.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-2 (cancelled)

Claim 3 (currently amended) The receiver as recited in claim [[2]] 6, wherein each of said plurality of first units comprises circuitry for receiving said particular phase of said clock signal and a complement of said particular phase of said clock signal and said serial data.

Claims 4-5 (cancelled)

Claim 6 (currently amended) ~~The receiver as recited in claim 5,~~ A receiver comprising:

an oscillator outputting three or more phases of a clock signal; and

a retiming mechanism coupled to said oscillator having circuitry for receiving said phases of said clock signal and serial data, and circuitry operable to reduce timing uncertainties in said serial data by outputting a value of said serial data sampled at a particular phase of said clock signal;

wherein said retiming mechanism comprises a plurality of first units, wherein each of said plurality of first units comprises circuitry for sampling said serial data using a said particular phase of said clock signal;

wherein said retiming mechanism further comprises a plurality of second units, wherein each of said plurality of second units is associated with a particular first unit, wherein each of said plurality of second units comprises circuitry for

outputting the value of said serial data sampled by said associated first unit upon activation;

wherein a particular second unit of said plurality of second units is activated based on a logical state of each input to said particular second unit; and

wherein said logical state of each input is determined based on combinational logic using said phases of said clock signal and complements of said phases of said clock signal.

Claims 7-8 (cancelled)

Claim 9 (currently amended) The system as recited in claim [[8]] 12, wherein each of said plurality of first units comprises circuitry for receiving said particular phase of said clock signal and a complement of said particular phase of said clock signal and said serial data.

Claims 10-11 (cancelled)

Claim 12 (currently amended) ~~The system as recited in claim 11,~~ A system comprising:

a transmission medium;

a transmitter coupled to said transmission medium configured to convert parallel data to a serial form; and

a receiver coupled to said transmission medium, wherein said receiver comprises:

an oscillator outputting three or more phases of a clock signal; and

a retiming mechanism coupled to said oscillator having circuitry for receiving said phases of said clock signal and serial data, and circuitry operable to reduce timing uncertainties in said serial data by outputting a value of said serial data sampled at a particular phase of said clock signal;

wherein said retiming mechanism comprises a plurality of first units, wherein each of said plurality of first units comprises circuitry for sampling said serial data using said particular phase of said clock signal;

wherein said retiming mechanism further comprises a plurality of second units, wherein each of said plurality of second units is associated with a particular first unit, wherein each of said plurality of second units comprises circuitry for outputting the value of said serial data sampled by said associated first unit upon activation;

wherein a particular second unit of said plurality of second units is activated based on a logical state of each input to said particular second unit; and

wherein said logical state of each input is determined based on combinational logic using said phases of said clock signal and complements of said phases of said clock signal.